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CORRELATING TEMPLATE PROPERTIES WITH THE QUALITY OF EPITAXIALLY GROWN SILICON WAFERS

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ABSTRACT: Epitaxially grown silicon wafers (EpiWafers) are a promising alternative to conventional wafers. High lifetimes are already reported for EpiWafers but still defects limit their quality. The properties of the reorganized porous silicon template affect the crystal defects in final EpiWafers. Therefore, the influence of reorganization temperature on template properties has been investigated. Atomic force microscopy (AFM) measurements reveal an increase of surface waviness of reorganized porous silicon layers with an increasing process temperature. A reduced distortion of the crystal lattice of the porous layers is measured for the higher temperature using high resolution X-ray diffraction (HRXRD). Though both properties have the potential for reducing the quality of subsequently grown epitaxial layers, measured defect densities and local minority charge carrier lifetimes suggest that there are other causes which are quality limiting. Thermal stress in combination with the mechanical weakness of the porous layers is identified as one decisive factor. Impurities in form of residual native oxide on pore walls are suspected to increase crystal defect formation as well.
Keywords: Epitaxy, Silicon Foil, porous Silicon

1 INTRODUCTION

In photovoltaics, the usage of epitaxially grown silicon wafers (EpiWafers) instead of common silicon wafers is beneficial in terms of energy consumption as well as material losses. Thus, the overall costs per watt peak can be reduced if the quality is comparable to conventional wafers. Good material quality of EpiWafers was already achieved. Minority charge carrier lifetimes of up to 9 ms are reported after a gettering step [1] and efficiencies of up to 23 % for solar cells made of EpiWafers [2]. The fabrication of EpiWafers requires a specific production sequence containing epitaxial growth of the final wafer on top of a reorganized porous silicon double layer that acts as template for growth and predetermined breaking layer for detachment. Since a high number of crystal defects currently limits the material quality of EpiWafers [3,4] a better understanding of the origin for crystal defect formation is essential for pushing forward the quality and thus the market-readiness of EpiWafers.

This contribution is dedicated to the investigation of reorganized porous silicon template characteristics and their impact on crystal defect formation. A deeper understanding of fundamental mechanisms proceeding during reorganization of porous silicon multilayers shall be gained, and it ought to be assessed whether the porous template causes crystal defect formation. Besides microstructural investigations based on scanning electron and atomic force microscopy (SEM and AFM), an extensive high resolution X-ray diffraction (HRXRD)-based analysis of the crystal structure of porous silicon multilayers and its strain states is examined. Crystal defect types, occurring in epitaxial silicon wafers are identified and their spatial distributions determined. A deeper understanding of the causes for defect formation and the correlation to investigated template characteristics is gained. Finally, recommendations for obtaining epitaxial silicon wafers of higher qualities are given.

2 EXPERIMENTAL PROCEDURE

2.1 EpiWafer fabrication

Highly boron doped substrates with an electrochemically etched porous silicon multilayer structure were provided by IMS (Institut für Mikroelektronik Stuttgart). The porous silicon multilayer structure has a low porosity layer (LPL) and a high porosity layer (HPL), consisting of two layers of slightly different porosities. The 6 inch samples were broken by hand to a size of 6 x 9 cm^2. The native oxide was removed with a HF dip before mounting the samples in a rapid thermal temperature chemical vapor deposition reactor (the RTCVD100) [5]. Samples were heated up with 150 K/min in hydrogen atmosphere till the final process temperatures of 1120 °C and 1220 °C were reached. Reorganization of porous silicon layers was carried out for 2 min. For the characterization of template properties, cooling was initiated with -100 K/min. EpiWafers were fabricated by epitaxial growth directly after reorganization at the same temperature for 17 min with a growth rate of about (4.4 $\pm$ 0.5) µm/min. The average layer thickness is 75 µm. No doping precursor was added leading to a Boron dopant concentration of around 6E14 cm^{-3}. Epitaxially grown layers were mechanically detached after defining the area of 40 x 50 mm^2 with a dicing saw, using an in-house developed lift-off tool. The residual porous silicon was removed by KOH etching (40 %) for 5 min at 80 °C resulting in final EpiWafers.

HF dipped polished Cz-wafers without porous silicon layers were used as reference substrates with best template properties for epitaxial growth. The resulting stack is called reference sample in the following.

Due to the reactor design of the RTCVD100, thermal induced bending of the samples with a radius of curvature between 46 m and 83 m occurs.

Crystallographic defects were visualized using Secco-etch [6] for 90 sec. Lifetime samples were passivated with Al_2O_3 by atomic layer deposition (ALD) on both sides after RCA cleaning.

2.2 Characterization

Structures within reorganized porous silicon layers were investigated on freshly broken cross sections by SEM.

The surface morphology of reorganized porous silicon samples was examined using AFM, operated in non-contact mode. At three different positions an area of 10 x 10 µm^2 was mapped with a lateral resolution of 256 x 256 pixel (≈ 39 nm). Root mean squared surface roughness values (R_q) were calculated from multiple line profiles, extracted from the measured area at an interval of 1 µm horizontally and vertically. From all obtained R_q-values, mean values and standard deviations were calculated.

Crystal structure investigations were carried out using a HRXRD setup operating with Cu K_α radiation (λ = 1.540598 Å). The system is equipped with a hybrid monochromator, consisting of a parabolic focusing mirror and a two-bounce Ge monochromator crystal. Scattered intensities were measured with a triple-axis setup. Reciprocal space maps (RSM) of the 004 and 224 Bragg reflections were recorded and in- (*a, b*) as well as out-of-plane (*c*) lattice parameters were extracted. In-plane lattice parameters are assumed to be equal ($a = b$). Allocation of a Bragg peak to a certain layer is based on relative intensities and layer thicknesses since the structure factors of porous silicon and silicon are expected to be similar.

Defect densities and their spatial distribution in EpiWafers as well as reference samples were determined with an optical light microscope and an automatized particle detection software on Secco etched samples.

Average lifetimes were determined on passivated EpiWafers by quasi steady state photo conductance decay (QSSPC) measurements and lifetime images were taken with a photoluminescence imaging (PLI) setup [7].

3 RESULTS AND DISCUSSION

3.1 Microstructure of reorganized porous silicon

Microstructural investigations were carried out on porous silicon layers, reorganized at 1120 °C and 1220 °C using SEM for cross sectional analysis and AFM for the examination of surface quality (see Figure 1).

After reorganization, a closed but slightly wavy surface developed. The LPL contains spherical pores, showing facets in parts, belonging to {100}, {110} and {111} families of planes. The HPL consist of two hollow layers with a massive silicon layer in between. Silicon pillars within the HPL form the connection of the massive silicon layer to the substrate as well as to the LPL.

Depending on the reorganization temperature, slight differences in the microstructure can be observed. Larger pores are formed at higher temperatures and faceting is more pronounced. Pore size distribution is quite homogeneous at 1120 °C with a tendency of smaller pores close to the HPL. At 1220 °C there is a distinct gradient in pore size from top to bottom. Close to the surface, very large pores have formed and mean pore distance is long. Pore size decreases towards the HPL and at the interface to the HPL, a second pore free region have formed. The massive silicon layer is less structured at 1220 °C compared to 1120 °C and less silicon pillars are present.

Surface texture is influenced by the reorganization temperature as well. AFM measurements in Figure 1 reveal that surface waviness is more pronounced for layers reorganized at 1220 °C ($R_q = (3.4 \pm 0.7)$ nm) compared to 1120 °C ($R_q = (\leq 0.2 \pm 0.2)$ nm). The value for the lower temperature is in good agreement with R_q values reported in literature for similar reorganization temperatures [8]. Surface waviness is related to pore distribution within the LPL as it is visible in the SEM images shown in Figure 1. Depressions at the surface are located above regions in the LPL which show a depletion of pores while hills are situated above very large pores by trend.

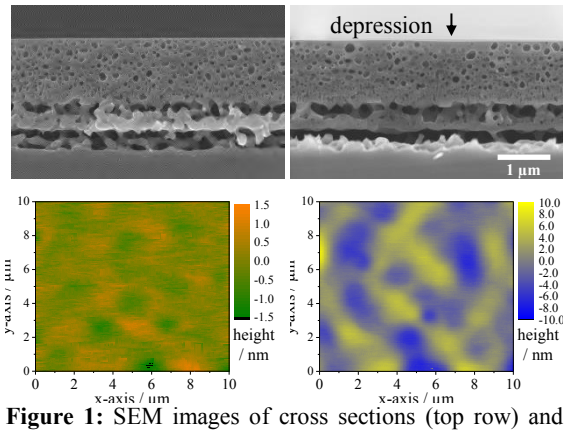

Figure 1: SEM images of cross sections (top row) and AFM measurements of surfaces (bottom row) of porous silicon layers reorganised at 1120 °C (left) and 1220 °C (right).

The microstructural evolution of porous silicon during reorganization can be explained based on the theory of sintering and is described in literature. The transformation of open trenches in as-etched porous silicon into faceted pores after reorganization is driven by energy minimization [9,10]. Energy gradients appear due to spatial distributed differences in free surface energy and differences in the residual stress fields around pores [11,12].

The above described differences in microstructure due to different reorganization temperatures coincide with results from literature [8] and could be due to different causes:

i) The mass flow during reorganization is based on surface and bulk diffusion of vacancies which is a thermal activated process [9]. Thus diffusion rate is temperature dependent and increases with higher temperatures.

ii) A prerequisite for surface diffusion of vacancies is the removal of the native oxide from the pore walls [13]. Incomplete de-oxidation of the pore walls at lower temperatures could hinder vacancy transport.

iii) Besides residual stress due to the porous nature of the layer, stress related to thermal expansion during annealing occurs which depends on temperature. Stress gradients have an influence on the structural evolution of pores which thus depends also on temperature [12].

The increased waviness at higher temperatures is a consequence of the pore size distribution within the LPL. Local depressions at the surface are located above pore free regions between large pores within the top part of the LPL. These pore free regions must be associated with a strong local removal of vacancies. Vacancy diffusion takes place between different pores due to the aforementioned energy gradients but is also directed towards the surface, which acts as a vacancy sink. As

pore distance increases, local diffusion of vacancies to the surface becomes more likely than to other pores. Thus between widely spaced large pores a local accumulation of vacancies arises at the surface, forming depressions.

The higher surface waviness at 1220 °C is a possible cause for crystal defect formation. Regarding the quality of EpiWafers, lower temperatures seem to be beneficial.

3.2 Crystal structure of reorganized porous silicon

HRXRD was used to record RSMs of 004 and 224 Bragg reflections of porous silicon multilayers in the as-etched state and after reorganization at different temperatures. In Figure 2, RSMs of as-etched porous silicon and reorganized porous silicon at 1120 °C (representative for all reorganized samples) are shown.

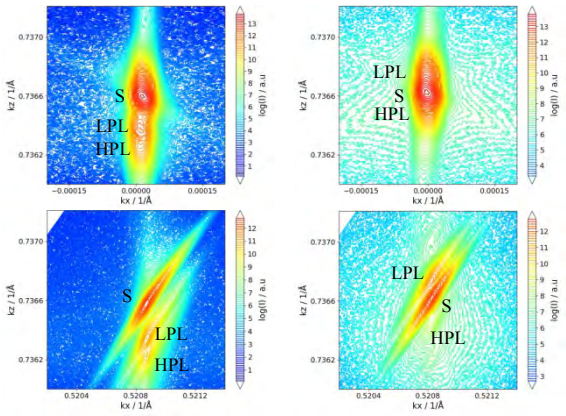

Figure 2: RSMs of 004 (top row) and 224 (bottom row) Bragg reflexions of porous silicon layers as-etched (left) and reorganized at 1120 °C (right).

Layers of different porosities form distinct Bragg peaks, shifted relative to the substrate peak in reciprocal space due to differences in the out-of-plane lattice parameter *c*. The in-plane lattice parameter *a* is equal for all layers and no tilt of any layer is observed. Thus, the crystal lattices of the porous layers are tetragonally distorted. Lattice parameters of all layers were extracted from the RSMs and are depicted in Figure 3.

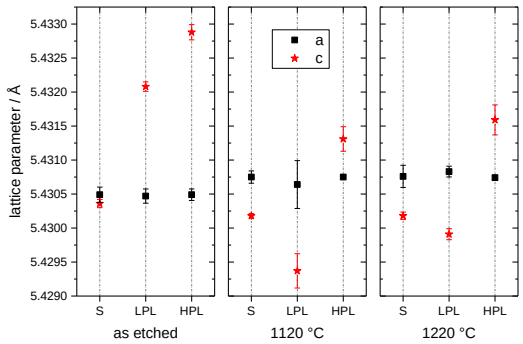

Figure 3: Lattice parameters extracted from RSMs for porous silicon as-etched (left) and reorganised at 1120 °C (middle) and 1220 °C (right).

In the as-etched state the porous layers exhibit an enlarged out-of-plane lattice parameter *c* compared to the substrate. The lattice parameter increases with increasing porosity. Comparable differences in lattice parameters between the porous layers and the substrate are also reported in literature [14].

After reorganization, lattice parameters change in all layers. The crystal lattice of the substrate gets distorted as well with a shortened out-of-plane lattice parameter *c*. The in-plane lattice parameter *a* is slightly increased compared to the as-etched state and hence the volume of the unit cell stays constant. The lattice distortion of the substrate can be explained by thermal induced bending of the entire sample after reorganization as mentioned in section 2.1. After reorganization, the strain state of the LPL is reversed compared to the as-etched state since *c* is smaller than *a*. This is not the case for the HPL where *c* is still larger than *a*, which is also the case for all porous layers in the as-etched state. With increasing temperature, strain decreases within the LPL and *c* gets larger. An increase in *c* with higher temperatures is also observed within the HPL but due do the opposite sign of the strain state (LPL: $c < a$; HPL: $c > a$), strain in the HPL increases at higher temperatures.

For the formation of strain, residual stress due to the huge inner surfaces of the porous layers as well as their chemical states play a key role. The reversal of the strain state of the LPL during reorganization can be explained by a change in surface termination with hydrogen or oxygen atoms of the pore walls [15]. In previous literature, no distinction is made between the layers of different porosities in porous multilayer samples concerning their strain states. The only hint for different strain states is based on cross sectional µ-Raman measurements, published in [16]. Accordingly, current models cannot explain why the strain state of the LPL is reversed after reorganization while this is not the case for the HPL. Possible causes are differences in the surface chemistry of the LPL and HPL but this has to be further investigated. Differences in preferred surface orientations are also expected to play a role, since stress acts perpendicular to the surfaces and thus influences the sign of strain. While in the as-etched state the surfaces of the open trenches in LPL and HPL are preferably vertically oriented, preferred surface orientations in the LPL and HPL differ after reorganization due to the different microstructure. Further, the porous nature of the layers might influence their thermal properties [17] leading to deviations in thermal stress within the LPL and HPL. Besides residual stress due to inner surfaces and their chemical state, thermal stress also influences the reorganization behavior of porous layers [12]. Though in general, strain induced by thermal stress is reversible after annealing, it might change the final strain state if plastic deformation took place during annealing. However, an unambiguous explanation for the observed evolution of strain has still to be given.

Strain in the porous layers and the associated difference in the out-of-plane lattice parameter *c* compared to bulk silicon is a possible source for crystal defect formation during epitaxy. Especially strain within the LPL might become important, since the LPL serves as template for epitaxial growth. Regarding strain in the LPL, higher process temperatures seems to be favorable for the template quality. This is contrary to an optimization of the surface quality of the template where lower temperatures are beneficial.

3.3 Crystal quality of epitaxial silicon wafers and correlations to template properties

The crystal quality of EpiWafers was investigated by measuring densities of different defect types, namely etch pits (EPs) revealing dislocations, stacking faults (SFs)

and polycrystalline inclusions bordered by stacking faults (pSF). EpiWafers processed at 1120 °C and 1220 °C were examined as well as epitaxial layers grown under same conditions on Cz-reference samples without porous layers.

Spatial distributions of the different defect types for all samples are depicted in Figure 4. Median defect densities and median absolute deviations are summarized in Table 1.

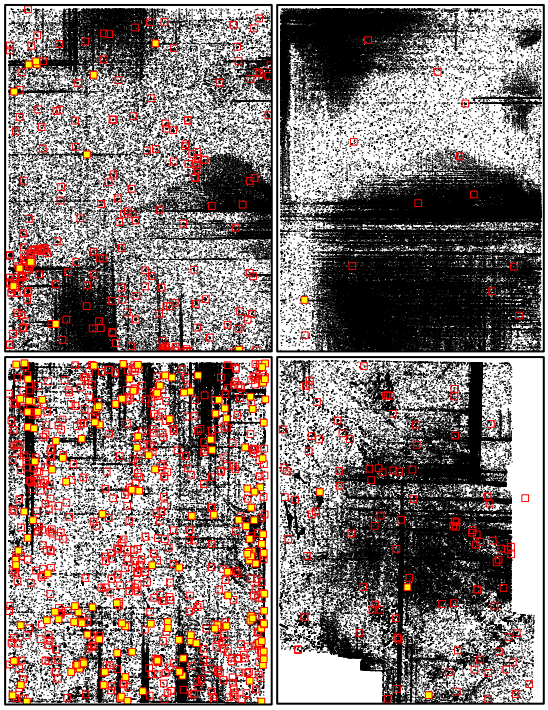

Figure 4: Distributions of EPs (blue dots), SFs (open red squares) and pSFs (yellow filled red squares) in 4 x 5 cm^2 reference samples (top row) and EpiWafers (bottom row) processed at 1120 °C (left) and 1220 °C (right).

SFs and pSFs are distributed over the entire area of the samples but occur more frequently in the outer regions. Only the EpiWafer processed at 1120 °C shows a significant amount of pSFs that have the most detrimental effect for lifetimes in EpiWafers [3,18]. The number of SFs in all samples exceeds the number of pSFs. EpiWafers show stacking fault densities (SFDs) which are multiple times higher than those on reference samples, processed under same conditions. Higher temperatures lead to a significant decrease in SFD in reference samples and EpiWafers.

The distribution of EPs can be divided into two classes:

i) a homogeneous distribution of etch pits with moderate local densities of about 3 x 10^3 cm^{-2} at 1120 °C and of about 8 x 10^3 cm^{-2} at 1220 °C on the entire area.

ii) local etch pit clusters which form a characteristic line pattern along <110> directions especially in EpiWafers. Bands of high local EPDs start from the rims of the samples and proceed towards the center region.

The distribution of these bands and their local EPD differ between EpiWafers and reference samples. Reference samples show larger areas of increased EPDs with local densities of up to 20 x 10^3 cm^{-2}. On EpiWafers are less bands of high EPDs but the local EPD within these bands is significant higher with values up to 35 x 10^3 cm^{-2}. With increasing temperature, the number of bands with high local EPDs increases in EpiWafers as well as in reference samples.

Table 1: Median densities of different defects in EpiWafers (EW) and reference samples (Ref).

Sample	**SFD / cm^{-2}**	**pSFD / cm^{-2}**	**EPD / 10^3 cm^{-2}**
EW, 1120 °C	29 ± 6	8 ± 3.0	5 ± 2
EW, 1220 °C	8 ± 5	< 0.1	10 ± 5
Ref, 1120 °C	6 ± 2	< 0.1	3 ± 1
Ref, 1220 °C	< 0.1	< 0.1	8 ± 3

In the following it is discussed whether the observed defect densities and their distributions can be explained by the investigated template properties.

Median EPDs are comparable between EpiWafers and reference samples, thus they are not related to characteristics of the porous silicon template like surface waviness or strain. The accumulation of etch pits along lines in <110> directions and the higher EPDs at higher temperatures is a clear indicator that dislocation formation is related to the formation of slip lines due to thermally induced strain [19]. At higher temperatures, the total thermal budget is higher due to a higher maximum temperature and longer heating times. Silicon also gets more ductile at higher temperatures which enable more plastic deformation. A correlation between thermally induced strain and the reactor design of the RTCVD100 is assumed. No slip lines have been observed in samples, processed in another CVD reactor (RTCVD160 [20]) by now, in which samples are vertically positioned and not horizontally on two fused silica bars as in the RTCVD100. Slip lines are observed in EpiWafers and in reference samples which is in good agreement with the observed bending of both sample types after processing. However, spatial distributions of slip lines and EPDs differ between both samples. This can be explained as follows: HRXRD measurements of samples containing a 5 µm thin epitaxial layer revealed a difference in orientation between the epitaxial layer and the substrate if the layer is grown on a porous silicon template. This is reflected in an additional Bragg peak within the 004 Bragg reflection which is shifted against the substrate peak along the ω-scan direction as shown in Figure 5. No such peak was observed in the RSMs of reorganized samples without epitaxial layer (Figure 2) or in RSMs of thin reference samples without porous silicon. This can be explained by the following model, graphically shown in Figure 5.

Thermal stress induces bending of the samples during processing, leading to plastic deformation and slip line formation. If stress becomes too high, mechanical failure partially occurs within the porous layer leading to a local detachment of the epitaxial layer and a difference in crystal orientation occurs. Due to the detachment, strain is released locally, leading to localized slip line formation with a very high local EPD. A strong indication for the occurrence of local detachment during growth is the formation of a crack at the vertex of the sample, filled with polycrystalline inclusions. In reference samples, no detachment of the epitaxial layer can take place due to the missing porous layers. This leads to a more homogeneous distribution of strain accompanied with the formation of a higher number of slip lines with lower

local EPDs compared to EpiWafers.

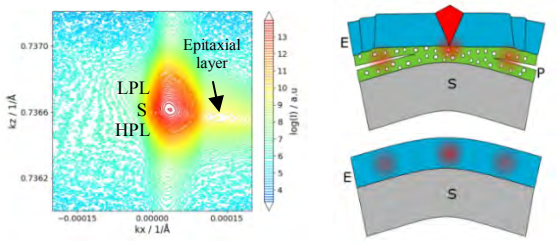

Figure 5: RSM of 004 Bragg reflexion of sample with 5 µm thin sample on reorganized porous silicon layer and substrate (left) and schemes of bowed samples after epitaxial growth with (top) and without (bottom) porous silicon with stress visualized in red. In edge regions in samples with porous silicon, growth of pSFs occurs as shown here. Closer to the centre stress is relieved by formation of agglomerated slip lines and accompanied by local detachment.

EpiWafers show higher median SFDs compared to reference samples and local SFDs are higher in the outer regions of all samples. According to literature, main causes for stacking fault formation are local impurities on the surface, e.g. a native oxide [21], on which nucleation centers are formed with an incorrect stacking sequence [22]. Reorganized porous silicon may contain higher amounts of residual native oxide than Cz-reference wafers since a complete removal of the native oxide at pore walls is difficult. Besides native oxide on the closed surface, native oxide at surface near pore walls might also be crucial for stacking fault formation. Incomplete removal of the native oxide in the outer regions of all samples could be caused by less de-oxidation because of poorer gas exchange. Lower temperatures at the outer regions due to the proximity to colder fused silica parts could also lead to enhanced stacking fault formation. At lower temperatures, the de-oxidation rate gets smaller [23]. Besides smaller de-oxidation rates, lower temperatures increase the nucleation density during epitaxy and island growth starts, rather than layer by layer growth [24]. Hereby the probability that nucleation starts on remnants of residual native oxide with an incorrect stacking sequence becomes higher. These explanations are in good agreement with the general trend of lower SFDs at higher temperatures at both sample types.

Impurities in form of particles are also discussed in literature to evoke stacking fault formation [3,25]. Though they might be responsible in parts for the observed stacking faults, it is unlikely that they lead to the characteristic distributions of stacking faults or the differences between EpiWafers and reference samples. Particle contamination is mainly related to sample handling and cleanliness within the CVD reactors, thus stacking fault distribution over the entire area should be random.

More relevant for solar cells than the pure crystal quality of the EpiWafers is the minority charge carrier lifetime which depends additionally on impurities within the samples. In the following, mainly the influence of template properties and resulting crystal defects on the local lifetime in EpiWafers is discussed.

3.4 Lifetime of EpiWafers

The effective lifetime of EpiWafers processed at the two different temperatures is depicted in Figure 6. Lines of low effective lifetimes (τ_{eff}) starting from the edges are visible on both samples, but a higher amount is visible on the sample processed at higher temperature. These lines correspond to the slip lines with high local EPDs described in the last section. They are more pronounced for the EpiWafer processed at the higher temperature as already discussed for the slip lines. Like the slip lines, these lines of increased recombination activity were not detected on samples processed vertically in the reactor RTCVD160 [18] and therefore are expected to be avoidable by a change of the reactor design. Besides the prominent lines, a higher density of dots with reduced lifetime can be found on the sample processed at lower temperature. These dots correspond to pSFs. Their detrimental effect on lifetimes in EpiWafers was already reported [3,18]. Additional lines in inner areas of the EpiWafers with a slightly reduced lifetime caused most probably by stress fields of pSFs are visible [18]. Beside the mentioned local reductions, an overall low lifetime is obtained with mean values of (22 ± 14) µs and (14 ± 9) µs for samples processed at 1120 °C and 1220 °C, respectively. The difference can partly be explained by the increased number of slip lines in the samples processed at higher temperature. As reported for the reactor RTCVD160 [26], metal impurities are probably the reason. The source of the overall reduced lifetime might dominate the local lifetime to an extend that avoids to see an impact of the SFD. A more detailed investigation of the recombination source is required.

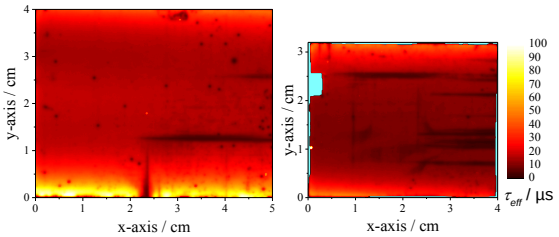

Figure 6: Lifetime images of EpiWafers fabricated at 1120 °C (left) and 1220 °C (right) measured by PLI at ≈1 sun equivalent illumination intensity.

4 CONCLUSION

Template properties of reorganized porous silicon layers, processed at different temperatures in the RTCVD100 were investigated using SEM, AFM and HRXRD. Though a closed surface develops on all reorganized samples, it shows a waviness which is more pronounced for higher temperatures. This is related to the characteristic microstructure in the surface-near regions of the LPL. An increase in pore size and pore distance at higher temperatures lead to enhanced vacancy diffusion to the surface and to the formation of local depressions. Though lower temperatures increase the template quality in terms of surface waviness, a loss of quality due to strain in the LPL is associated with lower temperatures. The origin for the evolution of strain in the porous layers are not finally understood but amount, orientation and chemical state of inner surfaces are the key points. Thus, improving the template quality in terms of surface waviness and strain by an optimized process temperature is in contradiction to each other.

In fact, defect densities and distributions in

EpiWafers and reference samples have revealed that surface waviness and strain are not the decisive quality limiting factors. SF formation is assumed to be mainly caused by remaining native oxide at the surface, especially of the pores. This becomes more severe at lower temperatures and thus SFD increases. The evolution of EPD with temperature is contrary to the evolution of SFD. Dislocation formation was found to be mainly related to thermal stress causing slip lines in the material during processing. At higher temperatures, EpiWafers are more prone to plastic deformation than reference samples due to the mechanical weakness of the porous layers. This leads to higher local EPDs in EpiWafers. These slip lines with high local EPDs are also visible in lifetime images as lines with increased recombination activity.

In summary, higher temperatures are beneficial for the quality of EpiWafers since the formation of SF and pSF can be reduced. However, care must be taken concerning the reactor design and the homogeneity of the temperature field. Since EpiWafers are very prone to plastic deformation during growth due to the porous layers of the template, thermal stress must be avoided as far as possible.

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