SELF-ALIGNED SELECTIVE EMITTER FOR PERC BASED ON INKJETABLE UV-POLYMER

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ABSTRACT: In this study, we investigate and demonstrate the general feasibility of a new approach for a self-aligned selective emitter process technology for passivated emitter and rear cell (PERC) technology based on inkjet printing of an UV-polymer ink in combination with plating for metallization. First, we present the major findings about the *single* process development of inkjet printing (*minimum printed structures of 36 µm*), emitter etch-back (*from R_{sh} = 80 Ω/sq to 144 Ω/sq with an etch time of 10 s*), low temperature passivation (*depositions temperatures of up to 250°C*), a lift-off process (*at elevated temperatures of 600°C*) and demonstrate that the UV-polymer ink shows sufficient chemical and thermal stability to the processes involved. Finally, the successful integration into the PERC process sequence with up-scaling to an industrial wafer size M2 and a first working cell device with an efficiency η = 19.68% is demonstrated. In comparison, a conventional mask&etch selective emitter approach using inkjet printing of an hotmelt ink in combination with a semi-automated enhanced alignment algorithm between inkjet and screen printing is processed in parallel showing η = 21.54% and a gain of $\Delta\eta$ = 0.16%$_{abs}$ compared to PERC cell with homogeneous emitter.
Keywords: PERC, selective emitter, inkjet printing, etching, passivation, lift-off, plating

1 INTRODUCTION

1.1 Motivation

The passivated emitter and rear cell (PERC) technology is meanwhile the standard technology in industrial production with a market share of approximately 63% according to ITRPV [1]. Thus, improving the conversion efficiency of PERC solar cells is of major interest and, according to simulations [2], can be improved by decreasing optical and electrical losses at the cell's front side by the integration of a selective emitter. Several technologies [3] are available in order to implement this architecture by *e.g.* mask&etch processes [4, 5], laser-assisted diffusion [6–8], and ion implantation [9, 10].

A key-enabler to decrease costs of the solar cell device is to decrease Ag-consumption. Moreover, new module and wafer sawing technologies enable a reduction in wafer thickness from 180 down to 140 µm, a higher yield of wafers per ingot, and, in turn, a second high potential in saving costs. Of course, this potential can only be exploited as the solar cell process is conducted with a low breakage rate. The presented new self-aligned emitter approach is completely contact-less for the front-side processing while using inkjet and Ni/Cu/Ag plating, hence, providing a suitable technology to realize a potential reduction in process costs.

1.2 Approach

The main advantage of a selective emitter structure is the reduction of surface recombination losses on the PERC front side and, thus, increasing the open circuit voltage potential V_{OC} of the solar cell. The saturation current density of an emitter j_0 represents the sum of all the recombination mechanisms inside the emitter. There are three regions of interest determining the recombination losses described in Fig. 1 (cross section P1): A lowly doped photoactive area j_{0e}, a highly doped photoactive area j_{0e+}, not covered by metallization due to alignment limitations, and a highly doped region in the metallized area j_{0met}.

Process route P1 as describes in Fig. 1 (left) can be optimized if alignment accuracy between the inkjet-defined selective emitter and the screen-printed metallization is improved [11, 12] but always depends strongly on the accuracy of the printing equipment and materials used.

In contrast, process route P2 in Fig. 1 (right), the self-aligned emitter approach, is totally avoiding a highly doped photoactive area j_{0e+} with only similar requirements to alignment accuracy as PERC cells with a homogeneous emitter.

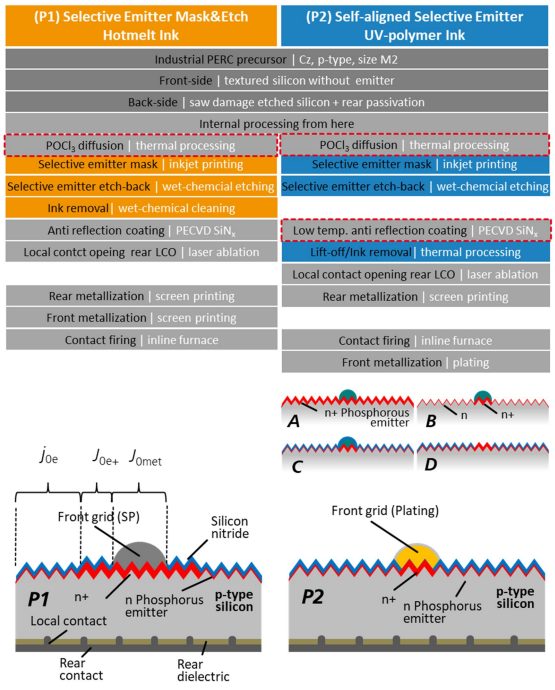

Figure 1: Process flow & cross section of two selective emitter PERC technologies based on industrial PERC precursors [13]. Additional process steps to a standard PERC route with homogenous emitter are highlighted by color. Dashed lines are indicating process adaptions

compared to standard.

For the self-aligned emitter (P2), the core processes are shown in Fig. 1 (A to D) starting with (A) printing of the UV-polymer ink as an etch mask on the textured silicon surface with a highly *n*-type doped emitter for the definition of the selective emitter. After the emitter etch-back (B) of the photoactive area, the ink is not removed, but remains on the surface during the deposition of the anti-reflection coating (C). Afterwards, a thermally triggered lift-off process (D) removes the ink and opens up the passivation only at the highly doped regions for a subsequent plating step.

Therefore this self-aligned emitter approach demands high requirements to the properties of the UV-polymer ink. As each process step (printing & UV-curing, etch-back, passivation, and lift-off) might influence ink properties like adhesion, ink structure, or its chemical or thermal stability; each process step has to be carefully evaluated. In the following, the development of the individual process steps will be explained, followed by the process integration into PERC solar cell and a discussion of the characteristic solar cell parameters.

2 PROCESS SET-UP AND DEVELOPMENT FOR SELF-ALIGNED EMITTER APPROACH

2.1 UV-polymer / hybrid ink

The UV-polymer ink is a hybrid ink developed by Sun Chemical. It is made out of two major components, which provides stability in the wet chemical and thermal treatment involved, while still allows to perform a feasible lift-off process for a subsequent plating step. In this work, we focus on a thermally triggered lift-off mechanism, but in principle other processes, as for example wet-chemical lift-off by dissolving or swelling, might be possible as well.

The first component is a hotmelt or wax that provides the chemical resistance to the solutions used for etch-back and surface cleaning. Furthermore, the hybrid ink is heated up to 90°C in order to be printable. When hitting the cold substrate, a phase change occurs and narrow line widths are possible, even on substrates with high surface energies. In addition, the wax is the volatile part of the ink to support the lift-off mechanism by sudden evaporation at elevated temperatures of around 600°C.

The second component is a UV curable polymer. Its main purpose is to provide the ink with thermal stability during the passivation process, and to capture the hotmelt component within the polymer mesh matrix until the lift-off process.

2.2 Printing & UV-curing

To evaluate and optimize printing performance, a PiXDRO LP50 laboratory printer from SUSS MicroTec with a custom-made print-head assembly featuring an industrial Canon C29 (formerly OCE Crystal Point) print-head with a nominal droplet volume of 29 pL and 256 nozzles and an air-cooled UV-LED (light emitting diode) system Powerline AC/IC 820 HP (wavelength: 395 nm) from Hoenle with irradiance of up to 16 W/cm^2 for *in-situ* UV-pinning is used. Due to the self-aligned nature, no sophisticated alignment procedure is necessary. In addition, the finger pitch can be easily adapted to the native resolution of the print-head itself, which allows single pass prints for all common wafer sizes and allows process times well below 1 s per wafer, as an array of print-heads is used accordingly.

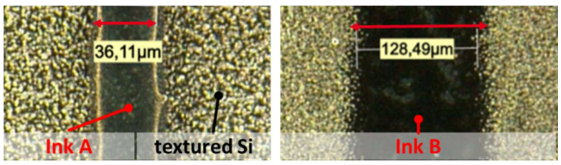

Figure 2: 2D microscopic pictures of two UV-polymer inks on textured silicon substrate after Printing, UV-pinning, and final UV-cure.

Several inks with different melting points of the hotmelt content as well as different ratios between hotmelt and UV-polymer content are tested. The optimized ink (Ink A in Fig. 2) shows the most narrow line width of 36 µm achieved after printing (700 dpi, printing speed of 250 mm/s), UV-pinning (intensity of 40 mJ/cm^2) and final UV-cure (3 passes at 350 mJ/cm^2). In contrast, ink B with a low melting point wax shows significant outbleeding compared to ink A, when using the same process parameters. Similar to hotmelt inks, a tight control of temperature (print-head, substrate, ambient and IR emission from the LED unit) is important.

2.3 Chemical resistivity against etch-back solution

For the selective emitter etch-back of the, a wet chemical batch process based on a HF:HNO_3:CH_3COOH:H_2O solution (volume fraction: 9:205:295:245) is used. The etch-back process flow, including the final cleaning step prior to front-side passivation, is described in Fig. 3.

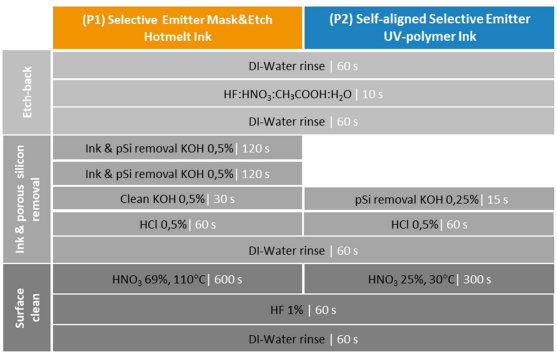

Figure 3: Detailed etch-back process flow showing the adaption of the conventional etch-back route (P1) to the self-aligned emitter approach (P2).

During the etch-back step, the uncovered crystalline silicon regions are transformed into a well-defined and homogeneous porous silicon layer (pSi) with a thickness of around 25 nm while using an etch-back time of 10 s. Then, the pSi-layer can be selectively removed by a low concentrated potassium hydroxide solution (KOH), because the etch rate of pSi is significantly higher than of crystalline silicon.

The removal of the hotmelt ink (P1) and pSi can be done simultaneously in a low concentrated KOH based stripping cascade. In addition, this avoids the usage of solvent based stripping solutions. Afterwards the surface cleaning procedure for hotmelt inks has no restriction as inks are previously removed and alternative cleaning procedures besides nitric acid (HNO_3) are applicable.

For the UV-polymer ink (P2), the KOH etch-time and

concentration has to be carefully adapted (0.25% KOH, 15 s) to maintain the ink structure on the surface during pSi removal. This adaption is necessary, as the hotmelt component is soluble in alkaline solutions and even captured within the UV-polymer mesh matrix, hence limiting the resistance to KOH. For the cleaning procedures concentration and temperature of the HNO_3 step has to be reduced according to the process flow in Fig. 3.

Fig. 4 demonstrates the homogeneous etch-back process until the edge of the printed lines. A perfect congruency between printed mask (Fig. 4 → A+B) and the selective emitter structure after ink removal (Fig. 4 → C) is achieved. For demonstration purpose, the pSi is not removed in order to be able to show sufficient contrast of etched and masked regions.

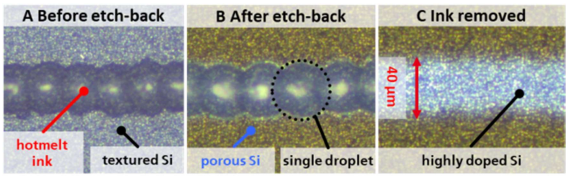

Figure 4: 2D microscopic pictures of hotmelt ink (P1) at certain process steps of the etch-back process.

The newest ink generations show sufficient adhesion to use single droplet lines and allow patterning with feature sizes of 40 µm for both process routes - P1 (hotmelt ink) and P2 (UV-polymer ink).

2.4 Thermal resistivity against PECVD-coated silicon nitride passivation

Typical industrial silicon nitride (SiN_x) deposition processes have temperatures in the range of 400°C, which is exceeding the thermal stability limit of the UV-polymer inks. Therefore, a low temperature SiN_x-PECVD process has to be evaluated using deposition temperatures between 150°C to 380°C. Results of this study are separately presented in a parallel paper from B. Kafle et al. at this conference [14], focusing on the optical and electrical properties of such layers. Here the thermal impact on the ink itself is briefly shown in Fig 5. The UV-polymer ink maintains its dome shaped structure until 250°C with a width of 52 µm. While exceeding this deposition temperature, shrinkage in line width to 48 µm occurs. Cracks are introduced, which becomes clearly visible for deposition temperatures of 380°C. The typical heat-up time for the full PECVD-process used in this study is 6 to 10 minutes. At deposition temperatures of 250°C, dwell times of up to 20 minutes have already been demonstrated to not have negative impact on the lift-off process.

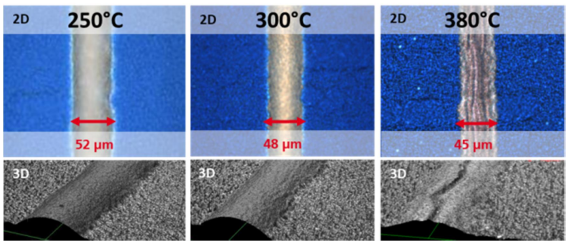

Figure 5: 2D (microscopy) and 3D (laser confocal microscopy) pictures of UV-polymer ink after PECVD-deposition at different deposition temperatures with contact dwell time (10 min).

2.5 Lift-off process

The thermally triggered lift-off process is done by placing the samples after PECVD deposition (Fig. 6 → A) on a hotplate at 600°C. A sudden evaporation of the hotmelt content is triggered, leading to the lift-off. After removing the samples from the hotplate (Fig. 6 → B), residues of the UV-polymer shell can still be observed. Those residues can be easily removed with a high pressure nitrogen gun (Fig. 6 → B), leaving only minor residues at the very edge of the opened line structure in some parts. Further variation in terms of temperature and duration already show some significant reduction of those residues and is part of ongoing investigations.

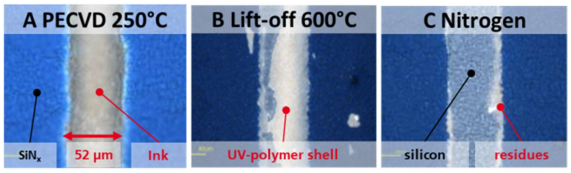

Figure 6: Microscopic pictures of the lift-off process after PECVD-deposition, lift-off process on hotplate, and post-treatment with high pressure nitrogen gun.

In Fig. 7 SEM/EDX-images (*scanning electron microscope / energy-dispersive X-ray spectroscopy*) are taken from samples after the lift-off process to determine if any SiN_x is present or might have penetrated the ink during deposition. In the centre, where the ink was lifted, a strong silicon signal is present whereas only at the edges nitrogen can be detected and a SiN_x layer is still present. This is also visible in the SEM-image (Fig. 7 → left side).

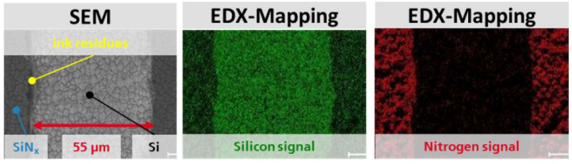

Figure 7: SEM/EDX-images of a sample after lift-off process with no traces of SiN_x, where the lift-off occurs.

3 PROCESS INTEGRATION

3.1 Experimental setup

After successful evaluation of the individual process steps the full process sequence is up-scaled to an industrial wafer size M2 and integrated into PERC fabrication according to the process flows and the industrial precursors described in Fig. 1 using the selective emitter etch-back process in Fig. 3. In Fig. 8, the different groups are briefly described.

(P1) Selective Emitter Mask&Etch Hotmelt Ink		(P2) Self-aligned Selective Emitter UV-polymer Ink	
1 Reference HE | SP30	2 SE100 | SP30	3 Reference HE | PL22	4 SE55 | PL60
Homogeneous emitter 95 Ω/sq	Selective emitter 80 Ω/sq / 144 Ω/sq	Homogeneous emitter 95 Ω/sq	Selective emitter 95 Ω/sq / 151 Ω/sq
	Hotmelt 100 µm	Laser Contact Opening 15 µm	Hybrid Ink 55 µm
Standard Passivation			Low Temperature 250°C
Screen Printing 30 µm/120 fingers		Plating 22 µm/115 fingers	Plating 60 µm/115 fingers

Figure 8: Group overview of the process integration experiment. Group coding: HE = homogeneous Emitter SE = selective emitter; SP = screen printing; PL= plating; digits = corresponding feature size in µm.

In total, the experiment consists of four groups. Two reference groups, group 1 and 3, with homogeneous standard emitter (HE) with a sheet resistance of 95 Ω/sq are added for both process flows in order to monitor the successful integration of the two selective emitter (SE) approaches.

For group 2 with the selective emitter approach P1 (hotmelt ink), an inkjet mask with a line width of 100 µm is printed on the textured silicon surface with a highly doped *n*-type diffused emitter with a sheet resistance (R_{sh}) of 80 Ω/sq. The emitter diffusion profile is adapted to the needs of the screen printing metallization in order to reduce contact resistance and recombination losses below the contact area (j_{0met}). It is followed by the etch-back process as described in Fig 3. The samples are etched in a HNO_3 based solution for 10 s and a final sheet resistance of 144 Ω/sq for the lowly doped photoactive area is reached. Afterwards, group 1 and 2 are simultaneously processed until contact firing.

For group 4 with the selective emitter approach P2, UV-polymer ink is printed on the textured silicon surface with an *n*-type emitter of 95 Ω/sq and a width of 55 µm, simultaneously defining the selective emitter and contact area for the following plating step. Afterwards, according to Fig. 3, the selective emitter is etched back for 10 s to a sheet resistance of 151 Ω/sq. After surface cleaning, a low temperature PECVD-passivation stack at a deposition temperature of 250°C is applied consisting of a thin (1-2 nm) thick plasma-oxide covered with a 78 nm silicon nitride on top. Finally, a state-of-the-art firing furnace is used with a constant temperature plateau at 600°C to trigger the thermal lift-off process. Residues are removed by a high pressure nitrogen gun. The reference group uses the same emitter, but without any etch-back step (R_{sh}= 95 Ω/sq), a typical high temperature passivation stack and laser contact openings with a width of only 15 µm. The remaining rear and front-side metallization processes are done simultaneously and no additional process adaption for group 4 has been applied.

3.2 Results and discussion

Table I: Parameters from STC current-voltage characterization. The cell tester measurements are performed using PCBtouch, thus, without busbars.

Group	η [%]	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]
1 HE | SP30	21.38	665.1	40.0	80.0
2 SE100 | SP30	21.54	670.8	40.1	80.1
3 HE | PL22	21.29	661.6	40.1	80.2
4 SE55 | PL60	19.68	638.8	38.6	79.9

The reference groups 1 and 3 with screen printed and plating metallization on homogeneous emitter reached efficiencies of 21.38% and 21.29%, respectively. This is in the expected range for the process sequence and material quality of the industrial precursors used within this experiment and indicates that all standard processes worked within their specifications.

Compared to group 1, group 2 with the selective emitter route P1 (hotmelt ink) using the sophisticated alignment procedure [11, 12] shows an efficiency gain of $\Delta\eta$ = 0.16%$_{abs}$ with the main benefit in the improved open circuit voltage (V_{OC}) of 5 mV. This demonstrates the general feasibility of the etch-back and alignment procedure used within the selective emitter route P1. To exploit the full potential of selective emitters, the diffusion profile in conjunction with improved homogeneity and fine-tuning of the etch-back process has to be further improved.

Group 4 is not yet matching the efficiency of the reference group 3 with major losses in V_{OC} and J_{SC}. Nevertheless, the demonstration of fully working devices at reasonable efficiencies should be considered a first big step for an innovative processing route with a very high potential. We conclude that even such a challenging, yet elegant, process route might become a viable option in the future after further optimization.

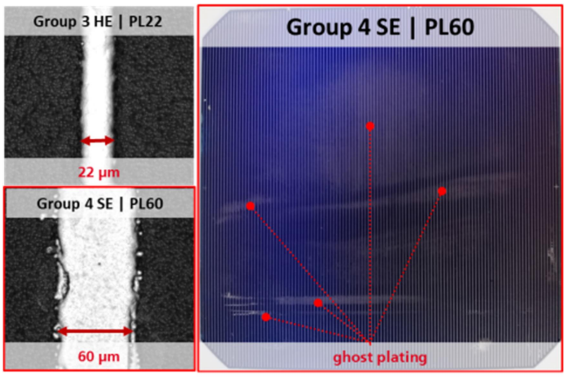

Figure 9: Left: Laser confocal microscopic images of plating metallization. Top: Group 3 with LCO. Bottom: Group 4 with lift-off. Right: Camera picture of a fully plated cell based on the presented self-aligned emitter technology.

The J_{SC} loss is mainly caused by the area fraction (A_{met}) of the metallization. Group 3 with 22 µm fingers (A_{met} = 1.6%) has significantly lower shading as group 4 with 60 µm (A_{met} = 4.4%) after lift-off and plating (see Fig. 9). This increased shading is responsible for almost 70% of the J_{SC} losses and accumulates to 1.07 mA/cm². The remaining 30% can be partially explained by a minor ghost plating behavior visible in Fig. 9 (wafer right side). Additional IQE/EQE measurements are planned to identify the remaining losses.

The low V_{OC} is only partially caused by the lower passivation quality of the low temperature passivation (LT) compared to the standard (high temperature) passivation (HT) as can be seen in Table II.

Table II: Emitter dark saturation current density j_{0e} for homogeneous (HE) and selective Emitter (SE) as diffused and after etch-back (SEe/HEe). Symmetrical life-time samples were processed according to their cell counterparts, measured with Quasi-steady-state photo conductance (QSSPC), and the data analyzed according to the slope method [15].

Group	1 HE	2 SEe	3 HE	4 HEe
Emitter		selective		selective
Passivation	HT	HT	HT	LT
R_{Sh} [Ω/sq]	95	144	95	151
j_{0e} [mA/cm²]	64	42	64	55

The Δj_{0e} = 9 mA/cm² between group 3 and group 4 in the photoactive area cannot fully explain the drop of >20 mV in V_{OC}. Assuming that the recombination below the plated contact is rather high (further analysis is still

pending), the increased fraction of the metallization (see Fig. 9) and ghost plating is the main source of the low V_{OC} values and the biggest lever to address the V_{OC} losses in the future.

The high fill factor *FF* almost 80%, comparable to the reference group 3 and the homogeneous response in electroluminescence measurement in Fig. 10 demonstrates that the core idea of this process route works and a homogenous plating result with sufficient low contact resistance over the full wafer area can be achieved.

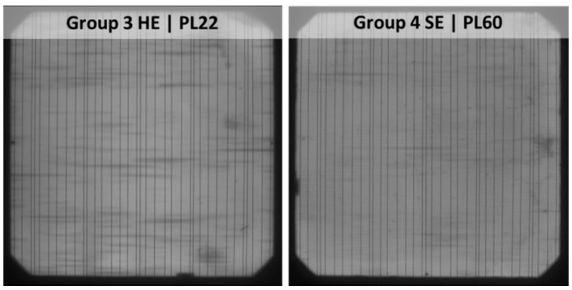

Figure 10: Electroluminescence (EL) picture of reference group 3 (left) and self-aligned emitter group 4 (right).

Therefore, further improvements should focus on the reduction of the printed line width from 55 µm down to ≤ 20 µm, e.g. by switching to print-heads with lower droplet volume ≤ 10 pL, and the evaluation of other low temperature (≤ 300°C) passivation technologies.

4 CONCLUSION & OUTLOOK

In this study, we successfully evaluated a new self-aligned emitter approach for PERC using a UV-polymer ink for inkjet printing in combination with a lift-off and plating process. Printed line widths down to 36 µm could be demonstrated with high printing speeds of 250 mm/s in a single print pass. Furthermore, the ink shows sufficient chemical and thermal resistance against the etch-back and passivation process. A full etch-back sequence with a HNO_3 based solution, shows excellent compatibility with the UV-polymer & hotmelt inks and allows short etch-back times of 10 s. No undercut can be observed. Furthermore the UV-polymer ink maintains its structure for PECVD deposition temperatures of up to 250°C for a duration of at least 20 minutes. An easy lift-off process could be demonstrated by simply placing a sample on a hotplate at 600°C for 10 minutes and a transfer to a state-of-the art firing furnace has been demonstrated on cell level.

For the first time, the full process sequence has been successfully integrated into a PERC process with efficiencies of up to 19.7%. Main losses in J_{SC} and V_{OC} can be attributed to the increased metallization fraction (shading) and ghost plating. The high fill factor *FF* of 79.9% and the homogeneous response in electroluminescence measurements demonstrate that the core idea of this approach works and is feasible for up-scaling.

The main lever for future improvements is the reduction of the metallization fraction by the utilization of print-heads with lower droplet volume. In addition the restriction to low temperature passivation schemes (≤ 250°C) is challenging, but atomic layer deposition for silicon passivation in a multi-functional stack might be a viable option.

Cell concepts with similar or less restrictions regarding deposition temperatures like selective TOPCon-structures or SHJ (-BCBJ) might be an interesting choice for future implementation, besides PERC.

In addition, a conventional mask&etch approach based on inkjet technology using hotmelt inks and screen printing metallization has been evaluated in parallel, demonstrating an efficiency of $\eta = 21.54\%$ and a gain of $\Delta\eta = 0.16\%_{abs}$ compared to their homogeneous emitter counterpart.

To exploit the full potential of selective emitters, the diffusion profile in conjunction with improved homogeneity and fine-tuning of the etch-back process has to be further improved.

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5 REFERENCES

[1] ITRPV, 2020, "International Technology Roadmap for Photovoltaic (ITRPV) - Results 2019,” 2019.

[2] P. Saint-Cast *et al.,* “Analysis of the losses of industrial-type PERC solar cells,” *Phys. Status Solidi A*, vol. 214, no. 3, p. 1600708, 2017, doi: 10.1002/pssa.201600708.

[3] G. Hahn and M. Z. Rahman, “Status of selective emitter technology,” in *25th EU PVSEC*, Valencia, 2010, pp. 1091–1096.

[4] T. Lauermann *et al.,* “Insect: An inline selective emitter concept with high efficiencies at competitive process costs improved with inkjet masking technology,” in *24th EU PVSEC*, Hamburg, 2009, pp. 1767–1770.

[5] S. Joonwichien, S. Utsunomiya, Y. Kida, M. Moriya, K. Shirasawa, and H. Takato, “Implementation of selective emitter for industrial-sized PERCs using wet chemical etch-back process,” *IEEE J. Photovoltaics*, vol. 8, no. 3, pp. 703–709, 2018, doi: 10.1109/JPHOTOV.2018.2806838.

[6] J. Weber, S. Lohmüller (neè Werner), E. Lohmüller, S. Wasmer, J. Nekarda, and A. A. Brand, “Simulations on laser-phosphorous-doped selective emitters,” in *7th World Conference on Photovoltaic Energy Conversion*, Waikoloa, Hawaii, 2018, 3588 - 3592.

[7] J. Weber, S. Gutscher, S. Lohmüller, E. Lohmüller, and A. A. Brand, “Laser-Doped Selective Emitter - Process Development and Speed-Up,” in *35th EU PVSEC*, Brussels, Belgium, 2018, 379 - 384.

[8] R. Müller *et al.,* "Evaluation of implantation annealing for highly-doped selective boron emitters suitable for screen-printed contacts," *Sol. Energy Mater. Sol. Cells*, pp. in press, 2013, doi: 10.1016/j.solmat.2013.06.040.

[9] H. Hieslmair, L. Mandrell, I. Latchford, M. Chun, J. Sullivan, and B. Adibi, "High Throughput Ion-Implantation for Silicon Solar Cells," *Energy Procedia*, vol. 27, pp. 122–128, 2012, doi: 10.1016/j.egypro.2012.07.039.

[10] E. Lohmüller *et al.,* "High-precision alignment procedures for patterning processes in solar cell production," *Prog. Photovolt: Res. Appl.*, vol. 28, no. 3, pp. 189–199, 2020, doi: 10.1002/pip.3218.

[11] R. Keding et al., "Precise Selective Doping and Metallization for Next-Generation PERC Technology," in *SNEC 13th, Shanghai (CN), 2019*.

[12] M. Müller, F. Wolny, G. Fischer, A. Krause, P. Palinginis, H. Neuhaus, "Change of the Bulk Carrier Lifetime of High Quality Silicon Wafers during PERC Solar Cell Processing," in *35th EU PVSEC*, Brussels, Belgium, 2018, pp. 366–370.

[13] B. Kafle et al., "Technological Viability and Proof-of-Concept of Applying Low-Temperature PECVD SiNx for Inkjet-Masked Selective Emitters," *in 37th EU PVSEC*, 2020.

[14] D. E. Kane and R. M. Swanson, "Measurement of the emitter saturation current by a contactless photoconductivity decay method (silicon solar cells)," in *18th IEEE Photovoltaic Specialists Conference Las Vegas*, Las Vegas, 1985, pp. 578–583.